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**BlueTiger™ Connected Optical Drive Family**  
**CD-84 and CD-88 CD Boards**

**Data Sheet version 1.0**

**June 2020**

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**Abstract**

Describes the CD-80 Commercial and Technical Specification.

**Document History**

No.	Primary Author(s)	Description of Version	Date Completed
V1.0	MJI	Initial version	04-06-2020

**Related Documentation**

Part Number	Description
CD-84_88_SW_CI	CD_84_88_SW_Command_Interface_Spec
PB_CD-84	BlueTiger CD-84 Product Brief
PB_CD-88	BlueTiger CD-88 Product Brief
JPL-2800	JPL-2800 tray loading mechanism specification
JPSL-33	JPSL-33 slot loading mechanism specification
DM-3381	DM3381 mechanism specification

**Ordering Information**

Part Number	Description	remark
CD-84-MB CD Board	CD-84 PCB	single 7.5V supply
CD-88-MB CD Board	CD-88 PCB	single 7.5V supply

**Release Notice**

This document is under configuration control and updates will only be issued as a replacement document with a new version number.

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## Preface

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### ***Warnings and Restrictions***

It is important to operate CD-84/88 within the specified input and output ranges described in this document. Exceeding the specified input/output ranges may cause unexpected operation and/or irreversible damage to your development system. If there are questions concerning the input/output ranges, please contact a company representative prior to connecting the input power. Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to your development system.

### ***If You Need Assistance***

If you have questions regarding either the use of this software command interface or the information contained in the accompanying documentation, please contact StreamUnlimited Optical Storage.

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## Introduction

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This document specifies the Commercial and Technical Specification of the CD-84 and CD-88 boards. Both are for use in the high end audiophile CD segment.

CD-84/88 contains the complete CD servo and decoder frontend (NXP SAA7824) with power driver (AMTEK AM5810FM) and an onboard microcontroller (ARM7 based). Only D/A conversion, power supply and a simple front-board is required to build a high end CD player. There is also a SUOS-product; UFB-8X available with a 12-character VF-Display.

CD-84 is specifically designed to fit to the CD-Pro-8 high-end top loading mechanism, whereas CD-88 was intended as successor of the CD-80 board with the same board dimensions and connector positions.

The CD-88 board matches to following loaders and traverse mechanisms:

- StreamUnlimited JPL-2800 loader mechanism with DM3381 (SANYO SF-HD850 based mechanism)
- F8829 loader with DM3381.
- JPSL-33 slot-loading mechanism with DM3381

Since the circuit for CD-84 and CD-88 is nearly identical the can run with the same binaries.

The main differences between CD-80 and CD-84/88 are:

- The internal clock oscillator is now completely switched off when the Masterclock is set to extern, to avoid any interference between 2 nominally identical clock frequencies
- The boards have an on board EEPROM, which stores the loader selection, offers the possibility to set some audio functions like the use of the internal oversampling filter, different serial data formats, switching SPDIF off and set the clock accuracy for SPDIF (this should only be used if the Masterclock is set to extern and the accuracy is more than 50ppm), swichting the validity flag in SPDIF ON or OFF and set the de-emphasis to internal or external.
- The laser current is now being monitored during play and can be output for burn-in or diagnostic purposes
- The boards can output the detailed status of the CIRC decoder to measure the performance rather than depending on listening tests.
- The tray speed is now being controlled by a PWM signal and can be varied in finer steps.

## 1 Board Overview

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The Hardware and firmware is compatible to all loaders and traverse mechanism listed above. The configuration is done via the EEPROM setting. If there is no valid loader selection in the EEPROM the boards expects that the loader selection is sent by the host muC via the high level Software interface by the control board after startup (AC\_Set\_Loader command).

### Communication

CD-80 requires a host microcontroller to send high level commands and read back UI information. The formatting of the data read to fit the specific display used in the set has to be done in the host controller. For a list of command please refer to the “CD\_84\_88\_SW\_Command\_Interface” specification. All high level commands for a basic implementation of a high end CD player are available as well as a set of commands that allow a different implementation of a certain feature or even a new one. For example CD-84/88 does not have a command for a programmable A->B repeat, but such a function can easily be implemented in the host micro by reading the current time on disc at the position A and B and sending the command Goto\_Min\_Sec\_Frame on the disc to play and repeat the part between those positions.

Unlike CD-80 the communication utilizes standard UART protocol, I<sup>2</sup>C versions may become available later.

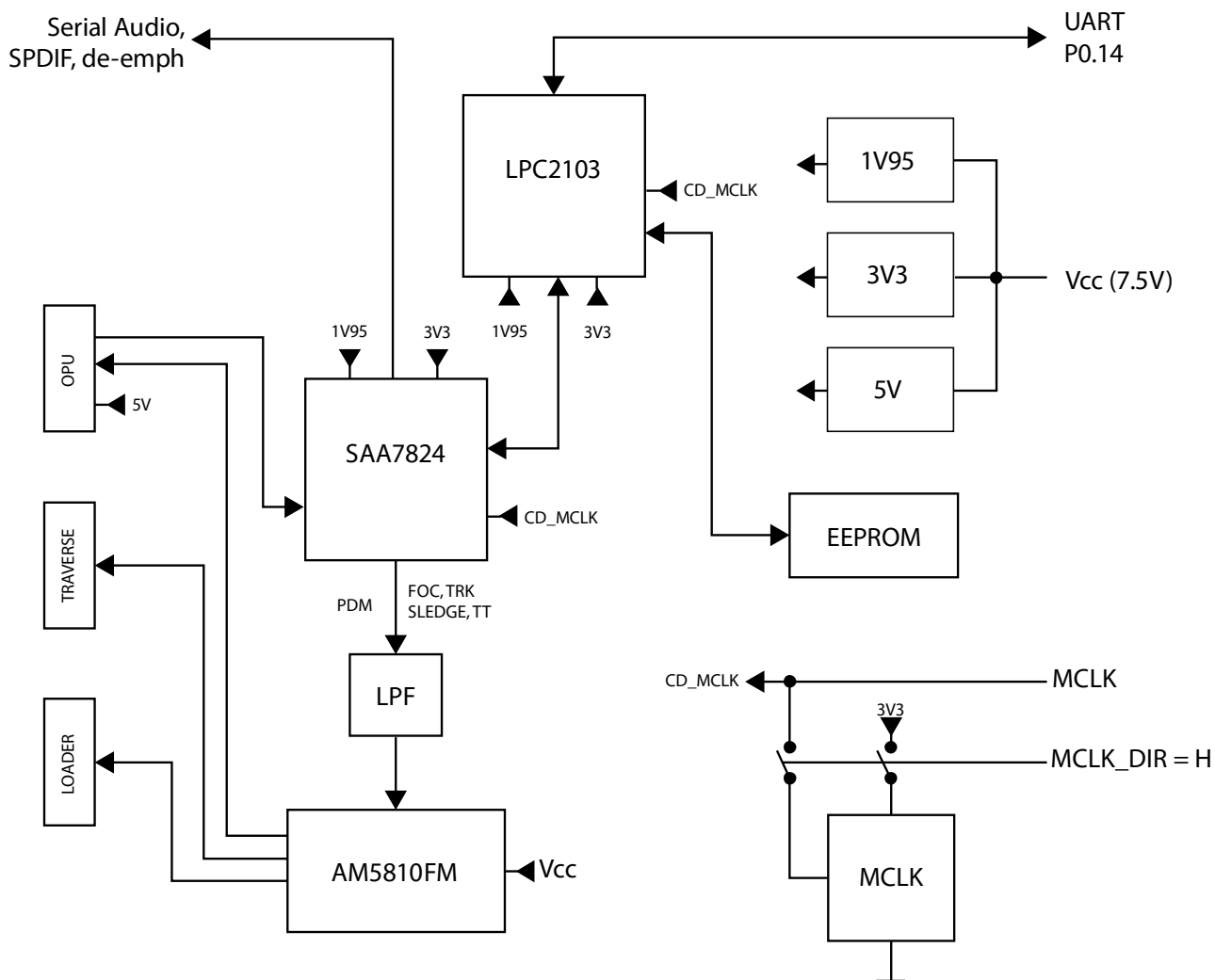
### Supported Loaders/OPU

Loader types:

- Tray Loader: JPL-2890 and F-8829
- Slot Loader: JP SL33
- Top Loading: CD-Pro8 or DM-3381

## 2 Block Diagram/System Architecture

Fig.1 Blockdiagram (standard version)

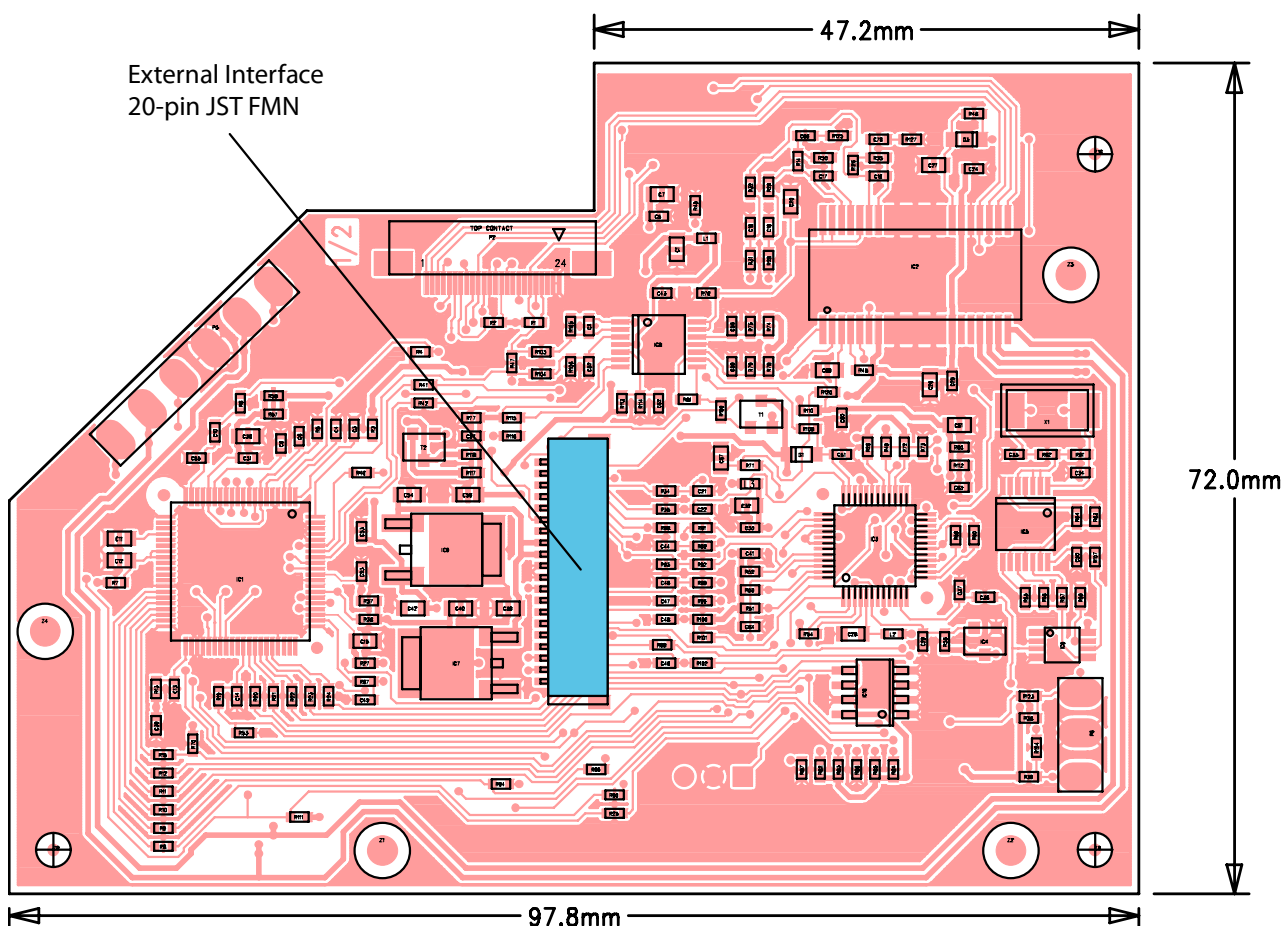


### 3 Physical specification

The PB is a two-layer board in single sided reflow soldering. The material is UL certified FR4. Capacitors and resistors prevail in 0603 dimension.

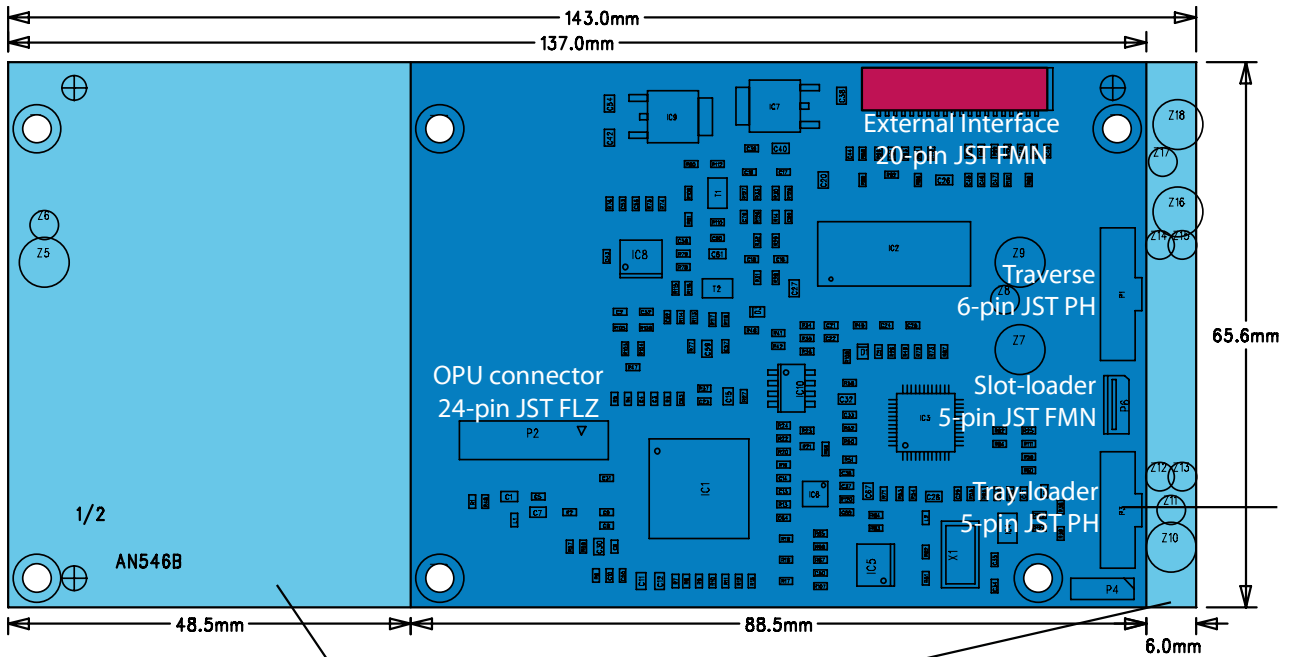
The finished and stuffed CD-80 module is in compliance with European Community Directive 2002/95/EC (RoHS) and Chinas law “Administration on the Control of Pollution Caused by Electronic Information Product” (ACPEIP, sometimes referred to as “China RoHS”)

#### 3.1 Dimensions CD-84





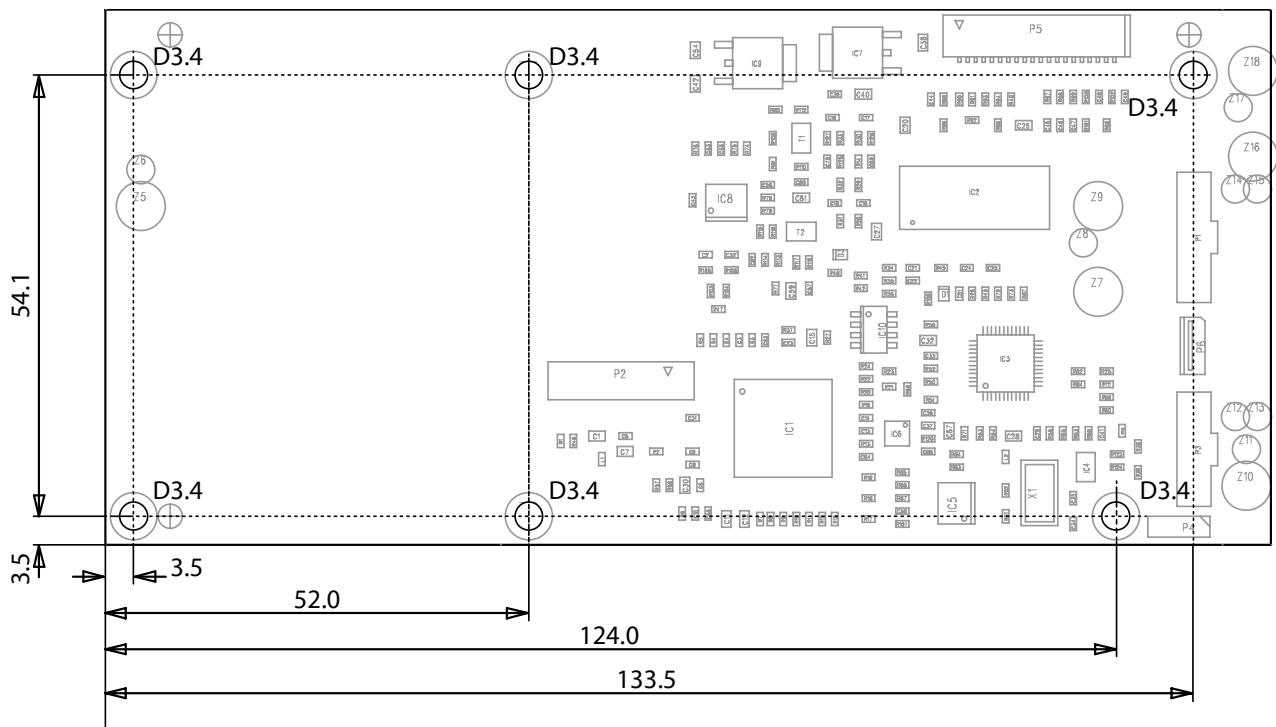
### 3.2 Dimensions CD-88



The PCB parts here shown in light blue, are prepared to be broken away

The bigger breakaway part on the left is for mechanical compatibility with CD-80 and the parts smaller part on the right is – as in CD-80 – to be used for mounting the board to the JPL-2800.

### 3.3 Mounting Holes CD-88

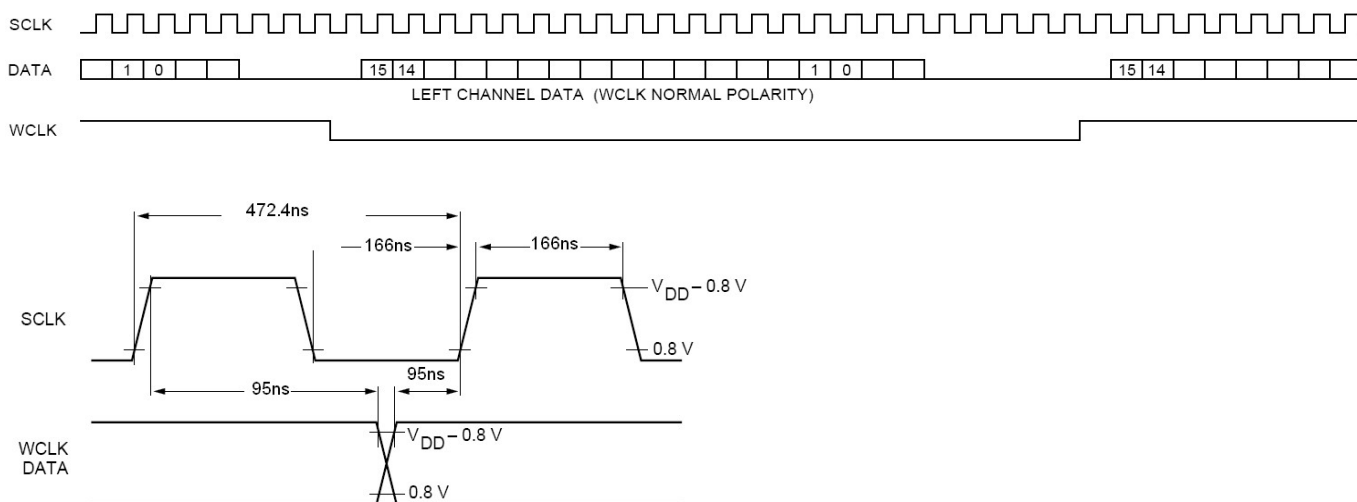


### 3.4 Interfaces

#### 3.4.1 Signal specifications

LVTTTL	<p>Low voltage transistor-transistor logic (3.3V logic)</p> <p>Caution: Exceeding the absolute maximum rating will cause damage to the board.</p>	<p>Absolute maximum rating:  <math>V_{IN} = -0.5V</math> to <math>3.8V</math>  <math>V_{OUT} = -0.5V</math> to <math>3.8V</math>                      Maximum current drive: 4mA</p> <table border="1"> <thead> <tr> <th>Parameter</th> <th>Min</th> <th>Max</th> </tr> </thead> <tbody> <tr> <td><math>V_{IH}</math> (V)</td> <td>2.0</td> <td>-</td> </tr> <tr> <td><math>V_{IL}</math> (V)</td> <td>-</td> <td>0.8</td> </tr> <tr> <td><math>V_{OH}</math> (V)</td> <td>2.4</td> <td>-</td> </tr> <tr> <td><math>V_{OL}</math> (V)</td> <td>-</td> <td>0.4</td> </tr> </tbody> </table>	Parameter	Min	Max	$V_{IH}$ (V)	2.0	-	$V_{IL}$ (V)	-	0.8	$V_{OH}$ (V)	2.4	-	$V_{OL}$ (V)	-	0.4
Parameter	Min	Max															
$V_{IH}$ (V)	2.0	-															
$V_{IL}$ (V)	-	0.8															
$V_{OH}$ (V)	2.4	-															
$V_{OL}$ (V)	-	0.4															
UART	RX and TX are LVTTTL level	57600 Baudrate 8/N/1															
I <sup>2</sup> C	Inter-IC All I <sup>2</sup> C signals at the board's connectors are LVTTTL levels.	[I <sup>2</sup> C_SPEC]															
I <sup>2</sup> S	Inter-IC Sound All I <sup>2</sup> S signals at the board's connectors are LVTTTL levels.	see below timing for details.															

#### I<sup>2</sup>S timing



### 3.4.2 Connector types and wiring requirements

Connector	Type	Max wiring length
external interface	FFC 20-way 1mm pitch side entry top contact	200mm
Slot loader	FFC 5-way 1mm pitch top entry	250mm
Tray loader	PH 5-way top entry	250mm
Traverse	PH 6-way top entry	200mm
CD OPU	FFC 16-way 1mm pitch side entry top contact	200mm

The 24pin flatfoil cable to the DVD pickup **must have the contacts** for **CD-84 on different sides**, connecting pin 1 of the OPU to pin 1 of CD-84 connector and For **CD-88 on the same side**, connecting pin 1 of the OPU to pin 24 of the CD-88 connector

### 3.4.3 External Interface connector

Pin	Assignment	Dir	Type	Description	internal pullup	logic
1	LPC_N_RST	IO	LVTTTL open drain	reset input/output (wired NOR)	4k7 to 3V3	low in reset
2	LKILL	O	5V tolerant open drain	kill output to improve SNR on digital silence track	none	high on silence
3	P0.14	I	LVTTTL	when pulled low during reset period, LPC microcontroller will be forced to HW bootloader for firmware upgrade	10K to 3V3	force low for upgrade
4	RKILL	O	5V tolerant open drain	kill output to improve SNR on digital silence track	none	high on silence
5	MUTE	O	LVTTTL push pull	mute output for audio board muting stages, mute remains active until TOC read and music reproduction starts	none	high to mute
6	DE-EMPH	O	LVTTTL push pull	this pin is only active if de-emph is set to external in the EEPROM. On tracks with de-emph the signal goes H	none	
7	GND	-	GND	global GND. All GNDs connected onboard		
8	VCC	I	POWER	supply. 7 – 10V, nominal 8V		
9	VCC	I	POWER	supply. 7 – 10V, nominal 8V		
10	GND	-	GND	global GND. All GNDs connected onboard		
11	GND	-	GND	global GND. All GNDs connected onboard		
12	SPDIF	O	LVTTTL	Digital out. Buffer needed for coax output	None	
13	SCL	I	LVTTTL	I <sup>2</sup> C clock input. 100kHz recommended. Only for I <sup>2</sup> C firmware build (not yet supported)	None	
13	RX	I	LVTTTL	CD-84/88 UART RX	10k to 3V3	
14	SDA	IO	LVTTTL	I <sup>2</sup> C data line. CD-80 is I <sup>2</sup> C slave. Only for I <sup>2</sup> C firmware build (not yet supported)	10k to 3V3	
14	TX	O	LVTTTL	CD-84/88 UART TX	10k to 3V3	
15	IRQ	O	LVTTTL	request line from I <sup>2</sup> C slave to I <sup>2</sup> C master. Only for I <sup>2</sup> C firmware build (not yet supported)	10k to 3V3	low for request
16	CD_LRCK	O	LVTTTL	Digital audio I <sup>2</sup> S – word clock, 44.1kHz		low for left
17	CD_SCK	O	LVTTTL	Digital audio I <sup>2</sup> S – bit clock, 2.11MHz		
18	MCLK	I/O	LVTTTL	Master clock input or output. 16.9344MHz		
19	CD_SDLR	O	LVTTTL	Digital audio I <sup>2</sup> S – data, 16/18bit, if not defined otherwise in EEPROM Audio Byte		
20	MCLK_DIR	I	LVTTTL	Masterclock direction	10k to L	L for OUT

### 3.4.4 DVD OPU Connector

Pin	Pin	Assignment	Direction	Type	Description
CD-88,	CD-84				
1	24	GND_LD	-	-	Laser diode Ground
2	23	DVD_LD	-	-	Connected to Ground
3	22	N/C	-	-	
4	21	N/C	-	-	
5	20	PD_MON	Input	Analogue	Laser Monitor Diode
6	19	CD_LD	Output	Analogue	CD Laser Diode
7	18	DVD_VR	-	-	
8	17	CD_VR	Input	Analogue	ALPC potentiometer for CD
9	16	N/C	-	-	
10	15	E	Input	Analogue	Satellite Diode 2
11	14	V <sub>cc</sub>	Output	Power	Power supply for OPU
12	13	V <sub>ref</sub>	Output	Power	Reference voltage for PD-IC
13	12	GND	-	-	OPU Ground
14	11	F	Input	Analogue	Satellite Diode 1
15	10	B/b	Input	Analogue	Central Diode B
16	9	A/a	Input	Analogue	Central Diode A
17	8	RF	Output	Analogue	RF signal
18	7	SW_DVD/CD	Output	-	Connected to V <sub>cc</sub>
19	6	D/d	Input	Analogue	Central Diode D
20	5	C/c	Input	Analogue	Central Diode C
21	4	TRK_NEG	Output	Power	Negative output of track actuator
22	3	TRK_POS	Output	Power	Positive output of track actuator
23	2	FCS_POS	Output	Power	Negative output to focus actuator
24	1	FCS_NEG	Output	Power	Positive output to focus actuator

## 4 Playability

### 4.1 Media

No	Media	Data type	Remark
5.1.1	CDDA	CD digital audio	Including CD text and "copy protected" CD
5.1.2	Hybrid SACD	CD layer	
5.1.3	CDR/CDRW	CD digital audio	

### 4.2 Test discs

No	Test disc	Item	Remark
5.3.1	SBC444A track 7	Wedge 600µm	No audible disturbances
5.3.2	SBC444A track 14	Black dot 600µm	No audible disturbances
5.3.3	SBC444A track 19	Fingerprint	No audible disturbances
5.3.4	Subchassis 8A track 8	Bad RF	No audible disturbances and fast searching check
5.3.5	Subchassis 8A track 15	Maximum read out diameter	Check the max. diameter read out performance.
5.3.6	Philips 8cm 0.6 deg skew disc tracks 1 and 6	Skew	Start up and play with the first 10mins. Check 4 positions each 90deg turned from the previous
5.3.7	TDC-732RA vertical deviation disc. First and last track	Vertical deviation	No failure during startup and play. Check 4 positions each 90 deg turned from the previous
5.3.8	Philips Eccentricity disc. First and last track	Eccentricity 150µm	No failure during startup and play. Check 4 positions each 90 deg turned from the previous
5.3.9	CDRW SBC444A track13	Black dot	No audible disturbances
5.3.10	CDRW SBC444A track17	Fingerprint	No audible disturbances
5.3.11	CDRW high reflection. First and last track	High reflection	No audible disturbances
5.3.12	CDRW low reflection. First and last track	Low reflexion	No audible disturbances

## 5 Application information

### 5.1 Power cycle timing

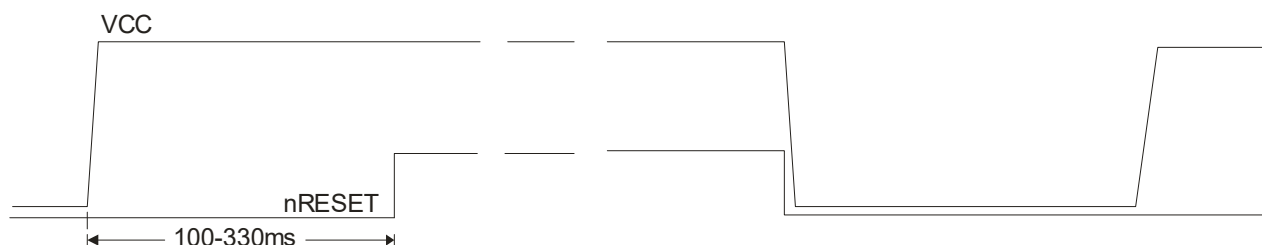
The CD-84/88 board operates in power-off and power-on mode only. There is no standby mode at board level. In power-off mode, the board does not respond to any communication or signals. As the pull-ups for the I<sup>2</sup>C bus are located on CD-80 board, it is not recommended to share the bus with other devices, which need to be powered while CD-80 is off.

Reset of the board is via an internal reset circuit, which is tied to the 3V3 supply. The reset will be activated immediately in case of a dip on VCC below about 5V. Note the delay at power on.

To reset the board externally, use an open drain output on nRESET line. It is recommended that host muC resets the CD-84/88 from time to time, to avoid that the state machines of the host and CD-84/88 get out of sync, in case that the set is being powered on for extended periods of time while the set is in stop mode.

After Power up the UART versions of CD-84/88 will send the EV\_READY\_FOR\_OPERATION. After this the board is ready to use.

Future I<sup>2</sup>C version will have the option to set the boards in the EEPROM to be compatible to CD-80. In this case the following timing applies:



### 5.2 Absolute maximum ratings

Voltage name	Mimimum input voltage ( $V_{ABSMIN}$ / V)	Maximum input voltage ( $V_{ABSMAX}$ / V)
8V	-0.5	12V

Note, that operating CD-84/88 at a supply more than 10V will not cause functional problems immediately, but causes thermal stress to the voltage regulators and the servo driver IC and should thus be avoided.

### 5.3 Power requirements

operation mode	average current consumption [mA]	peak current consumption [100ms measurement interval]
stop	200	
play	350	
open/close		500
track skip		1500

The supply concept is optimized for easy integration into a product. All GNDs are connected together on board level. If there is a separate power GND available in the application, it is beneficial to use pin 11 as digital GND.

### 5.4 Safety

CD-80 complies to IEC 60065 under following supply conditions:

8V level within specified range (7-10V)

8V current limited to 3A or less

for deviating supply conditions, the compliance has to be re-evaluated during product development

### 5.5 Muting concept, output data validity

CD-80 will output SPDIF signal as long as the supply is on.

When using internal Master Clock mode, the Master Clock will also be output permanently.

I2S signals are switched on after the first command has been received from the frontpanel (AC\_Set Loader). But during TOC reading of a disk, the I2S signals need to be switched to high impedance. If a disk is loaded, the I2S lines will become valid again when TOC has been read.

This method does not cause problems with most DACs, in case, the DAC used in the application produces some clicks when switching WCLK and SCLK signals off and back on, the mute line provided by CD-80 may be used to overcome any audible interference. See below diagram on signals for the case, that the unit is switched on with a disk loaded already, then the disk is removed and the tray; after trying to read the TOC without a disk loaded, the tray is opened and a new disk is loaded, TOC is being read and the disk is played.

Note: the mute line will be high impedance while the onboard microcontroller is in reset, so the line can be pulled high by an external logic at power on.

### 5.6 Operating temperature range

Performance specification valid for 25°C ambient temperature.

CD-80 will work between -10°C and 60°C.

Please note, that optical pickups used with CD-80 may have a lower operating temperature range, as the laser lifetime is highly dependent on temperature.

**6.1 EMC**

CD-84/88 will meet legal emission limits when used inside a metal application with reasonably sized openings for display etc. Main disturbance originates from the external Masterclock and I<sup>2</sup>S lines, so care has to be taken to reduce coupling of the cables and attached boards to the outside world and keep the 20pin flatfoil cable as short as possible which will also reduce crosstalk between the signals that pass over the flatfoil.

**6.2 ESD**

Although CD-84/88 board is not very critical w.r.t. ESD when operated in a finished product, special care has to be taken during assembly to avoid damage of either the board or the pickup of the mechanism.

The laser diode of a pickup is extremely sensitive to ESD when the connections are floating. This is especially relevant for a DVD pickup, where the laser is operated in pulsed mode and thus cannot be protected by a large capacitor in parallel on the pickup.

Following precautions thus must be taken when connecting a pickup to CD-80:

- Make sure, that the flatfoil to the pickup is inserted while the supply is off.
- Do not touch the exposed conductive strips of the flatfoil when inserting.
- ESD precautions have to be taken when touching the flatfoil, as there is a danger to damage the pickup laser.
- During transportation of the pickup and traverse, the laser is protected by a short circuit formed by a drop of solder on the pickup flexprint. As a DVD mechanism has two lasers, such pickups must have both lasers shorted during transportation either by two separated or a combined drop of solder. This solder drop must be removed AFTER connecting the flatfoil to CD-84/88 board. A soldering iron with the tip connected to ESD GND must be used for this purpose!